Curriculum Vitae

Dejan Ničković

AIT Austrian Institute of Technology GmbH.
Donau-City-Strasse 1
1220 Vienna,
Austria
Tel: +43 50550-4021
Email: Dejan.Nickovic@ait.ac.at

Personal Details:

Born on 30th January 1981
in Belgrade, Serbia
Serbian nationality
Single

Education

2004–2008	PhD at Verimag, University Joseph Fourier, Grenoble, France; Supervisor: Dr. Oded Maler; Subject: Timed and Hybrid Properties: Theory and Applications Defense in October 2008
1999–2003	Bachelor of Science (Honours), Information and Technology, University of Malta Stream: Computer Science, Mention: First Class Honours Dissertation (final year project): *Distributed Shared Variables for User-Level Fine-Grained Multithreading*; Grade: A+; Supervisor: Joseph Cordina

Employment

2011–	Scientist at Austrian Institute of Technology (AIT)
2009–2011	Post-doc at IST Austria, Klosterneuburg, Austria; Group of Prof. Thomas Henzinger
2008–2009	Post-doc at EPFL, Lausanne, Switzerland; Group of Prof. Thomas Henzinger
2007	Intern at Rembus, Inc.

2003–2004	Intern at Verimag, under the supervision of Dr. Oded Maler.
2000–2002	Part-time work in the Euro-Mediterranean Centre for Insular Coastal Dynamics (ICoD), Foundation for International Studies, St. Paul Street Valletta VLT 07, Malta, under the supervision of Anton Micallef.

Professional Interests and Skills

Professional Interests

- Formal verification and validation
- Formal specification and languages for validation
- Real-time modeling and analysis
- Embedded systems modeling and analysis
- Component-based modeling and analysis
- Property-based analysis and monitoring of analog and mixed-signal systems
- Time-triggered scheduling
- Distributed and concurrent models
- Controller synthesis

Skills

- Formal specification languages (temporal logic, SVA, PSL)
- Programming languages C, C++ and Java
- System-level UNIX programming in C
- SCADE, UML, MATLAB/Simulink, VerilogA

Professional Experience

Ongoing Projects

2014–2017	AIT Project Leader in the FFG Ikt der Zukunft Harmonia project
2014–2016	Coordinator of the European Defence Agency (EDA) Mistral project
2013–2016	Participation in the EU Crystal project
2011–2014	Participation in the EU Mbat project
2011–	Participation in the EU pSafeCer and nSafeCer projects

Past Projects

2011–2014	Participation in the Austrian Trufal project
2008-2011	Participation in the EU Combest project
2008–2011	Participation in EU Network of Excellence ArtistDesign
2004–2007	Participation in the EU project Prosyd

Teaching Activities

Spring 2009	Teaching assistant in course "Theoretical Computer Science" (EPFL). Course instructor: Prof. Tom Henzinger.

Professional Activities

Chair in Conferences, Workshops and Special Sessions

1. Tool and Publicity Chair at the 15th International Conference on Runtime Verification (RV), 2015.
2. Special Session Co-Chair on Model-based Analysis and Testing of Embedded Systems (MBAT) at the Second International Conference on Model-Driven Engineering and Software Dewelopment (MODELSWARD), 2014.
3. Program Co-Chair of the 10th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), 2012.
4. Chair of the Special Session on Robustness at the 6th IEEE International Symposium on Industrial Embedded Systems (SIES), 2011.

Program Committee Member

1. Program Committee member at the 15th International Conference on Runtime Verification (RV), 2015.
2. Program Committee member of the ERCIM/EWICS/ARTEMIS Workshop on Dependable Embedded and Cyber-physical Systems and Systems-of-Systems (DECSoS), 2014.
3. Program Committee member of the 2nd User Conference on Advanced Automated Testing 2014 (UCAAT), 2014.
4. Program Committee member of the 14th International Conference on Application of Concurrency to System Design 2014 (ACSD), 2014.
5. Program Committee member of Embedded Software Engineering (ESE) track in the 40th Euromicro Conference on Software Engineering and Advanced Applications (SEAA), 2014.
6. Program Committee member of ERCIM/ARTEMIS/EUROMICRO Special Workshop-Session on Teaching, Education and Training for Dependable Embedded and Cyberphysical Systems (TET-DEC), 2014.
7. Program Committee member of ERCIM/EWICS Workshop on Dependable Embedded and Cyberphysical Systems (DECS), 2013.
8. Program Committee member of Embedded Software Engineering (ESE) track in the 39th Euromicro Conference on Software Engineering and Advanced Applications (SEAA), 2013.

9. Program Committee member of the 11th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), 2013.

10. Program Committee member of the 7th IEEE International Symposium on Industrial Embedded Systems (SIES), 2012.

11. Program Committee member of the Conference on Frontiers in Analog Circuit Synthesis and Verification (FAC), 2011.

12. Program Committee member of the Fourth Workshop on Interaction and Concurrency Experience (ICE), 2011.

13. Program Committee member of the Eleventh International Conference on Application of Concurrency to System Design (ACSD), 2011.

14. Organizing Committee member of the 8th International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), 2010.

15. Program Committee member of the Third Workshop on Foundations of Interface Technologies (FIT), 2010.

16. Program Committee member of the Third Workshop on Interaction and Concurrency Experience (ICE), 2010.

17. Program Committee member of the Second Workshop on Interaction and Concurrency Experience (ICE), 2009.

18. Program Committee member of the Eight Workshop on Runtime Verification (RV), 2008.

External Reviewer

Book Chapters: Handbook of Model Checking, 2013.
Journals: ACM TOPLAS 2012, IEEE TCAD 2012, Information and Computation 2012, STTT 2012, TCAD 2012, Acta Informatica 2013.
Conferences and Workshops: FORMATS 2005, CAV 2008, FORMATS 2009, ACM SAC 2010, DATE 2010, FMCAD 2010, CAV 2011, FMCAD 2011, CAV 2012, FSTTCS 2012, MONTEREY 2012, RV 2012, LICS 2013, TACAS 2013, RV 2013, CAV 2014, FM 2014, PODC 2014, RV 2015, FSTTCS 2015, POPL 2015, SOFSEM 2015.

Publications

The order of the authors is in the alphabetical order in all the publications, except for C9, C17, TR1 and TR2 in which the authors are ordered by their contribution.

Invited Tutorials

T1 D. Ničković and R. Schlick. Model-based Testing for Safety Critical Systems. *Safety Day 2013*, FH Campus, 2013.

T2 J. Havlicek, S. Little, O. Maler, D. Ničković. Property-Based Monitoring of Analog and Mixed-Signal Systems. In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2010.

Invited Talks

I1 D. Ničković. Monitoring Mixed Signal Assertions - Theory, Tools and Applications. In *6th Workshop on Frontiers in Analog CAD (FAC)*, 2014.

I2 D. Ničković. Time for Mutants. In *First Workshop on Formal and Informal Methods for Correctness and Performance (FIMCP)*, 2013.

I3 D. Ničković, T. Henzinger, A. Legay, B. Delahaye and U. Fahrenberg. Incremental Time-triggered Scheduling. In *First International Workshop on Model-based Design with a focus on Extra-Functional Properties (MBDEFP)*, 2011.

I4 D. Ničković. Monitoring properties of AMS designs. *Rigorous Embedded Design (RED)*, 2011.

Refereed Journal Papers

J1 O. Maler and D. Ničković. Monitoring Properties of Analog and Mixed-Signal Circuits. In *Software Tools for Technology Transfer (STTT)*, 2013.

J2 K. Jones, V. Konrad and D. Ničković. Analog Property Checkers: A DDR2 Case Study. In *Formal Methods in System Design (FMSD)*, 2010.

Refereed Conference and Workshop Papers

C1 B. Aichernig, K. Hörmaier, F. Lorber, D. Ničković, R. Schlick, D. Simoneau and S. Tiran. Integration of Requirements Engineering and Test-Case Generation via OSLC. In *14th International Conference on Quality Software (QSIC)*, 2014.

C2 T. Nguyen and D. Ničković. Assertion-based Monitoring in Practice - Checking Correctness of an Automotive Sensor Interface. In *19th International Workshop on Formal Methods in Industrial Critical Systems (FMICS)*, 2014.

C3 T. Nguyen and D. Ničković. Monitoring Correctness of DSI3 Sensor Interfaces in a Modern Airbag System-on-Chip Application. In *6th Workshop on Frontiers in Analog CAD (FAC)*, 2014.

C4 P. Daca, T. Henzinger, W. Krenn and D. Ničković. Compositional Specifications with IOCO. In *7th IEEE International Conference on Software Testing, Veriication and Validation (ICST)*, 2014.

C5 W. Krenn, D. Ničković, L. Tec. Efficient Test-Case Generation For Compositional Real-Time Specifications. In *11th International Conference for Software Quality, Test and Innovation (ASQT)*, 2013.

C6 W. Krenn, D. Ničković, L. Tec. Incremental Language Inclusion Checking for Networks of Timed Automata. In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2013.

C7 B. K. Aichernig, F. Lorber and D. Ničković. Time for Mutants - Model-based Mutation Testing with Timed Automata. In *7th International Conference on Tests and Proofs (TAP)*, 2013.

C8 T. Henzinger and D. Ničković. Independent Implementability of Viewpoints. In *MONTEREY*, 2012.

C9 A. Donzé, O. Maler, E. Bartocci, D. Ničković, R. Grosu and S. Smolka. On Temporal Logic and Signal Processing. In *10th International Symposium on Automated Technology for Verification and Analysis (ATVA)*, 2012

C10 B. Delahaye, U. Fahrenberg, T. Henzinger, A. Legay and D. Ničković. Time-triggered Scheduling and Synchronous Interfaces. In *IFIP International Conference on Formal Techniques for Distributed Systems joint international conference: 14th Formal Methods for Open Object-Based Distributed Systems and 32nd Formal Techniques for Networked and Distributed Systems (FMOODS/FORTE)*, 2012.

C11 E. Asarin, A. Donzé, O. Maler and D. Ničković. Parametric Identification of Temporal Properties. In *2nd International Conference on Runtime Verification (RV)*, 2011.

C12 T. Henzinger, D. Ničković, N. Piterman, A. Tomar, M. Vardi and J. Fischer. Dynamic reactive modules. 2011. In *Proc. Concurrency Theory (CONCUR)*, 2011.

C13 D. Ničković and N. Piterman. From MTL to Deterministic Timed Automata, In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2010.

C14 L. Doyen, T. Henzinger, A. Legay and D. Ničković. Robustness of Sequential Circuits, In *Proc. Application of Concurrency to System Design (ACSD)*, 2010.

C15 O. Maler, D. Ničković and A. Pnueli. Checking Temporal Properties of Discrete, Timed and Continuous Behaviors, In *Pillars of Computer Science*, 2008.

C16 K. Jones, V. Konrad and D. Ničković. Analog Property Checkers: A DDR2 Case Study. In *Workshop on Formal Verification of Analog Circuits (FAC)*, 2008.

C17 D. Ničković and O. Maler. AMT: A Property-based Monitoring Tool for Analog Systems, In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2007.

C18 O. Maler, D. Ničković and A. Pnueli. On Synthesizing Controllers from Bounded-Response Properties, In *Proc. Computer Aided Verification (CAV)*, 2007.

C19 O. Maler, D. Ničković and A. Pnueli. From MITL to Timed Automata. In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2006.

C20 O. Maler, D. Ničković and A. Pnueli. Real Time Temporal Logic: Past, Present, Future. In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2005.

C21 O. Maler and D. Ničković. Monitoring Temporal Properties of Continuous Signals. In *Proc. Formal Modelling and Analysis of Timed Systems (FORMATS)*, 2004.

Edited Volumes

E1 Marcin Jurdzinski, Dejan Ničković (Eds.): **Formal Modeling and Analysis of Timed Systems - 10th International Conference, FORMATS 2012, London, UK, September 18-20, 2012. Proceedings.** Lecture Notes in Computer Science 7595, Springer 2012.

Technical Reports

TR1 Albert Benvenise, Dejan Ničković and Thomas Henzinger, Compositiional Contract Abstraction for System Design, *Raport de recherche RR-8460 INRIA*, 2014.

TR2 Albert Benveniste, Benoît Caillaud, Dejan Ničković, Roberto Passerone, Jean-Baptiste Raclet, Philipp Reinkemeier, Alberto Sangiovanni-Vincentelli, Werner Damm, Thomas A. Henzinger, Kim G. Larsen. Contracts for System Design, *Rapport de recherche RR-8147 INRIA*, 2012.

TR3 D. Ničković and N. Piterman. From MTL to Deterministic Timed Automata, *Technical Report 2009/2 Imperial College London*, 2009.

Miscellaneous

M1 D. Ničković. Checking Timed and Hybrid Properties: Theory and Applications, *PhD Thesis*, 2008.

Tools

MoMuT::SCADE

Tool for mutating SCADE models, implemented in Java.
http://www.ait.ac.at/momut/

MoMuT::TA

Tool for mutation-based test case generation from networks of timed automata models, implemented in Java and Z3.
http://www.ait.ac.at/momut/

AMT

Tool for property-based monitoring of analog and mixed-signal simulation traces, implemented in C++, using Qt and Qwt libraries.
http://www-verimag.imag.fr/DIST-TOOLS/TEMPO/AMT/content.html

RobusT

Tool for checking robustness of digital components, implemented in Java.
http://www.combest.eu/home/?link=tools&featureid=0&toolid=6

Summer schools

17th International School for Computer Science Researchers, Formal Methods: Theory And Practice, Lipari, Italy, 2005.

Languages

English	Fluent
French	Fluent
Italian	Good
Serbian	Mother language
Greek	Fair
Spanish	Fair
German	Beginner

Contacts for Reference

Dr. Manfred Gruber

Head of Safe and Autonomous Systems (SAS) Business Unit, AIT
Vienna, Austria

Email address: Manfred.Gruber@ait.ac.at

Prof. Thomas Henzinger

President of IST Austria
Klosterneuburg, Austria

Email address: tah@ist.ac.at

Dr. Oded Maler

Research Director in CNRS
Verimag, Grenoble, France

Email address: Oded.Maler@imag.fr

Prof. Kevin Jones

City University London
(previously at Rambus, Inc.)

Email address: Kevin.Jones.1@city.ac.uk